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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,622	01/28/2004	Pei-Jei Hu	JCLA11981	5650

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EXAMINER	
COLEMAN, VANESSA V	
ART UNIT	PAPER NUMBER
2627	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,622	HU ET AL.	
	Examiner	Art Unit	
	Coleman, Vanessa	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/8/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 10-12* is/are rejected.

7)☒ Claim(s) *4-9 and 13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Specification

The disclosure is objected to because of the following informalities: In line 6 of [0019] and line 17 of [0020] the term "detail" should read "detailed." Also, in line 8of [0019] the phrase "where the SyncFnd locate in the SyncWin" should read, "where the SyncFnd is located in the SyncWin." Finally line 6 of [0020] (page 9) describes both a clock generator and a clock signal with "EFMCLK."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Jang et al. (hereafter "Jang"), US Patent 6,536,011.

Regarding Claim 1, Jang discloses a method of correcting a clock of a compact disk, comprising; receiving a data signal (Fig. 12, RD_IN) and a clock signal (RD_CLK) (Col. 7, lines 15-18 and lines 35-36); generating a sync pattern signal (SYNC_FOUND) by using the clock signal to detect the data signal (Col. 7, lines 35-37); generating a detection window signal (SYNC_WIN) according to a clock number (RD_CNT) during a timing of a last sync pattern signal and a first preset timing (Col. 7, lines 66-67 and Col. 8, lines 42-49, where the limitation "a first preset timing" is met by "the expected timing of the sync detection signal") the detection window signal having a second preset timing width (Col. 8 lines 42-45); and comparing a clock of the sync pattern signal with the detection window signal, and correcting the clock signal (Col. 8, lines 8-16, where the limitation "comparing a clock of the sync pattern signal with the detection window signal" is met by lines 13-16, since the SYNC_FOUND signal must be generated within a time of the SYNC_WIN signal to avoid generating a PSYNC_FOUND signal, thereby a comparison of the sync pattern signal with the detection window signal; the limitation "correcting the clock signal" is met by lines 8-11, as the PSYNC_FOUND is generated to correct the clock.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. US Patent 6,536,011 (hereafter "Jang"), in view of Lee, US Reissued Patent RE37,904 E (hereafter "Lee").

Regarding Claim 10, Jang discloses a circuit for correcting a clock of a compact disk, comprising: a synchronous detecting circuit (Fig. 12, Sync Pattern Detector 130), adapted to receive a clock signal (RD_CLK) and a data signal (RD_IN) for generating a sync pattern signal (SYNC_FOUND) by using the clock signal to detect the data signal (Col. 7, lines 15-18 and lines 35-36); detection window generator (SYNC WINDOW GENERATOR 150), for generating a detection window signal (SYNC_WIN) according to a clock number (RD_CNT) during a timing of a last sync pattern signal and a first preset timing (Col. 7, lines 66-67 and Col. 8, lines 42-49, where the limitation "a first preset timing" is met by "the expected timing of the sync detection signal") the detection window signal having a second preset timing width (Col. 8 lines 42-45); and a

synchronous phase detecting circuit (Sync Pattern Detector 130), for comparing a clock of the sync pattern signal with the detection window signal, and (Col. 8, lines 8-16, where the limitation "comparing a clock of the sync pattern signal with the detection window signal" is met by lines 13-16, since the SYNC_FOUND signal must be generated within a time of the SYNC_WIN signal to avoid generating a PSYNC_FOUND signal, thereby a comparison of the sync pattern signal with the detection window signal; the limitation "generating a frequency-correcting signal according to the compare result for correcting the clock signal" is met by lines 8-11, as the PSYNC_FOUND is the frequency-correcting signal).

Jang does not disclose that the detection window generator is adapted to receive the clock signal and the sync pattern signal; or that the synchronous phase detecting circuit is adapted to receive the sync pattern signal and the detection window signal.

Lee discloses a detection window generator (Fig. 10, "window processing means 125") that is adapted to receive a clock signal ("clk1") and a sync pattern signal ("Isync") (Col. 5, lines 33-37); and a synchronous phase detecting circuit (Fig. 9, "final block sync signal detecting means 126") that is adapted to receive a sync pattern signal ("Bsync1") and a detection window signal (Col. 5, lines 61-63; Col. 5 36-37).

It would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the apparatus of Jang with the window processing means 125 and the final block sync signal detecting means 126 of Lee in order to generate a window with appropriate timing with respect to the sync pattern signal and to insure

processing of accurate sync pattern signals. Jang and Lee are analogous art because they both involve processing of digital data.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (hereafter "Jang"), US Patent 6,536,011 in view of Yokogawa (hereafter "Yokogawa"), US Patent 5,065,384.

Regarding Claim 2, Jang discloses the method of base claim 1, but does not disclose wherein the sync pattern signal is generated when the clock signal and the data signal change from zero to non-zero simultaneously.

Yokogawa discloses a method of correcting a clock of a compact disk, wherein the sync pattern signal (Fig. 4, "sync-signal detection signal b") is generated when the clock signal ("reproducing clock signal e") and the data signal ("edge pulses a") change from zero to non-zero simultaneously (Col. 1, lines 54-68, Col. 2, lines 1-2, and Col. 4 lines 5-9; where the "detected signal edge" of the RF signal that comprise the "edge pulses a" are understood to correspond to a change from zero to non-zero or non-zero to zero of the RF signal. In order for the reproducing clock signals e to be accurately counted by the synchronism detection circuit 4, "the edge pulses a" and "reproducing clock signal e" must be synchronized, thereby changing from zero to non-zero simultaneously. It is understood that the synchronism detection circuit 17 of the later

disclosed invention performs this process when detecting a sync-signal detection signal i.)

It would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the apparatus of Jang with synchronism detection circuit 17 of Yokogawa in order to determine that a sync-signal (sync pattern signal) with correct space is detected a predetermined number of times so as to generate a proper detection window signal.

Regarding Claim 3, Jang discloses the method of base claim 1, but does not disclose wherein the sync pattern signal is generated when the clock signal and the data signal change from non-zero to zero simultaneously.

Yokogawa discloses a method of correcting a clock of a compact disk, wherein the sync pattern signal (Fig. 4, "sync-signal detection signal b") is generated when the clock signal ("reproducing clock signal e") and the data signal ("edge pulses a") change from non-zero to zero simultaneously (Col. 1, lines 54-68, Col. 2, lines 1-2, and Col. 4 lines 5-9; where the "detected signal edge" of the RF signal that comprise the "edge pulses a" are understood to correspond to a change from zero to non-zero or non-zero to zero of the RF signal. In order for the reproducing clock signals e to be accurately counted by the synchronism detection circuit 4, "the edge pulses a" and "reproducing clock signal e" must be synchronized, thereby changing from zero to non-zero simultaneously. It is understood that the synchronism detection circuit 17 of the later

disclosed invention performs this process when detecting a sync-signal detection signal i.)

It would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the apparatus of Jang with synchronism detection circuit 17 of Yokogawa in order to determine that a sync-signal (sync pattern signal) with correct space is detected a predetermined number of times so as to generate a proper detection window signal.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (hereafter "Jang"), US Patent 6,536,011 and Lee, US Reissued Patent RE37,904E (hereafter "Lee"), in view of Yokogawa, US Patent 5,065,384 (hereafter "Yokogawa").

Regarding Claim 11, Jang and Lee disclose the circuit of base claim 10, but do not disclose wherein the sync pattern signal is generated when the clock signal and the data signal change from zero to non-zero simultaneously.

Yokogawa discloses a method of correcting a clock of a compact disk, wherein the sync pattern signal (Fig. 4, "sync-signal detection signal b") is generated when the clock signal ("reproducing clock signal e") and the data signal ("edge pulses a") change from zero to non-zero simultaneously (Col. 1, lines 54-68, Col. 2, lines 1-2, and Col. 4 lines 5-9; where the "detected signal edge" of the RF signal that comprise the "edge pulses a" are understood to correspond to a change from zero to non-zero or non-zero

to zero of the RF signal. In order for the reproducing clock signals e to be accurately counted by the synchronism detection circuit 4, the "edge pulses a" and "reproducing clock signal e" must be synchronized, thereby changing from zero to non-zero simultaneously. It is understood that the synchronism detection circuit 17 of the later disclosed invention performs this process when detecting a sync-signal detection signal i.)

It would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the apparatus of Jang and Lee with synchronism detection circuit 17 of Yokogawa in order to determine that a sync-signal (sync pattern signal) with correct space is detected a predetermined number of times so as to generate a proper detection window signal.

Regarding Claim 12, Jang and Lee do not disclose the circuit of base claim 10, but do not disclose wherein the sync pattern signal is generated when the clock signal and the data signal change from non-zero to zero simultaneously.

Yokogawa discloses a method of correcting a clock of a compact disk, wherein the sync pattern signal (Fig. 4, "sync-signal detection signal b") is generated when the clock signal ("reproducing clock signal e") and the data signal ("edge pulses a") change from non-zero to zero simultaneously (Col. 1, lines 54-68, Col. 2, lines 1-2, and Col. 4 lines 5-9; where the "detected signal edge" of the RF signal that comprise the "edge pulses a" are understood to correspond to a change from zero to non-zero or non-zero to zero of the RF signal. In order for the reproducing clock signals e to be accurately

counted by the synchronism detection circuit 4, "the edge pulses a" and "reproducing clock signal e" must be synchronized, thereby changing from zero to non-zero simultaneously. It is understood that the synchronism detection circuit 17 of the later disclosed invention performs this process when detecting a sync-signal detection signal i.)

It would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the apparatus of Jang and Lee with synchronism detection circuit 17 of Yokogawa in order to determine that a sync-signal (sync pattern signal [illegible]) with correct space is detected a predetermined number of times so as to generate a proper detection window signal.

Allowable Subject Matter

Claims 4-9 and 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the references of record, alone or in combination disclose or suggest the method or apparatus of base claims 1 and 10, further including defining a signal front-edge, a signal post-edge, a front-edge region, and a post-edge region of a window detection signal, where the step of comparing the clock of the sync pattern signal with the detection window signal further comprises determining in what region of the detection window signal the sync pattern signal is and sending out either a frequency-increase, frequency-reduction, or frequency- remain signal and correcting the clock signal according to these signals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Galbraith et al.	US 5,255,132
Karino, Shingo	US 5,677,935
Tonami et al.	US 7,050,363 B2
Yamanoi et al.	US 6,269,058 B1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vanessa Coleman whose telephone number is (571) 272-9081. The examiner can normally be reached on 8:30-6 M-T; Off 1st Friday; 8:30-5 2nd Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER